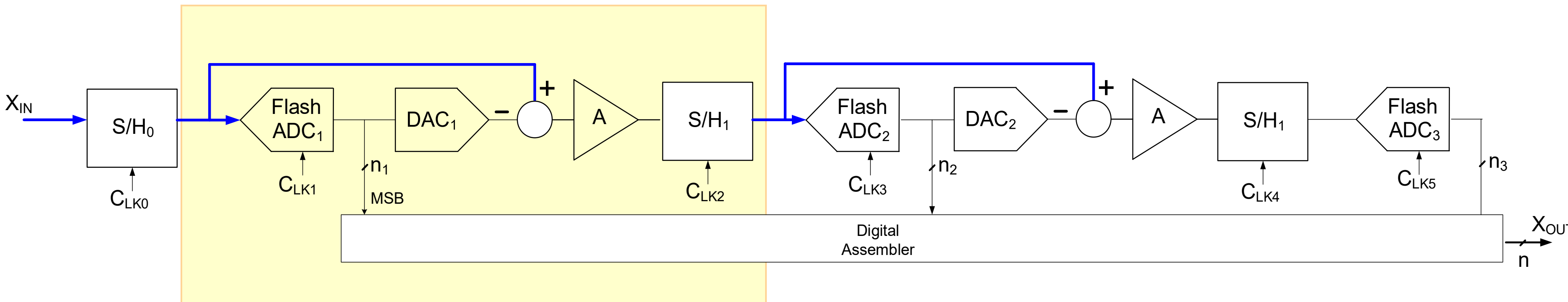
EE 435

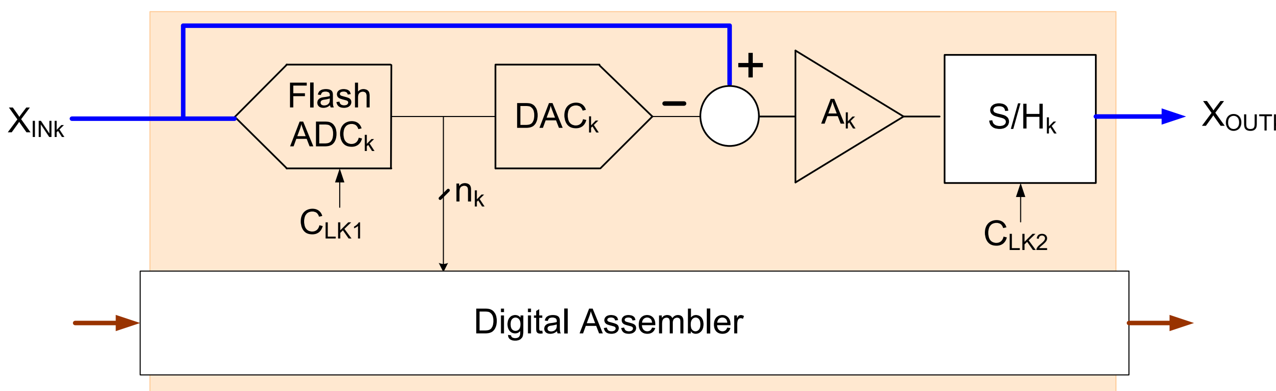
Lecture 37

ADC Design

Review from Last Lecture

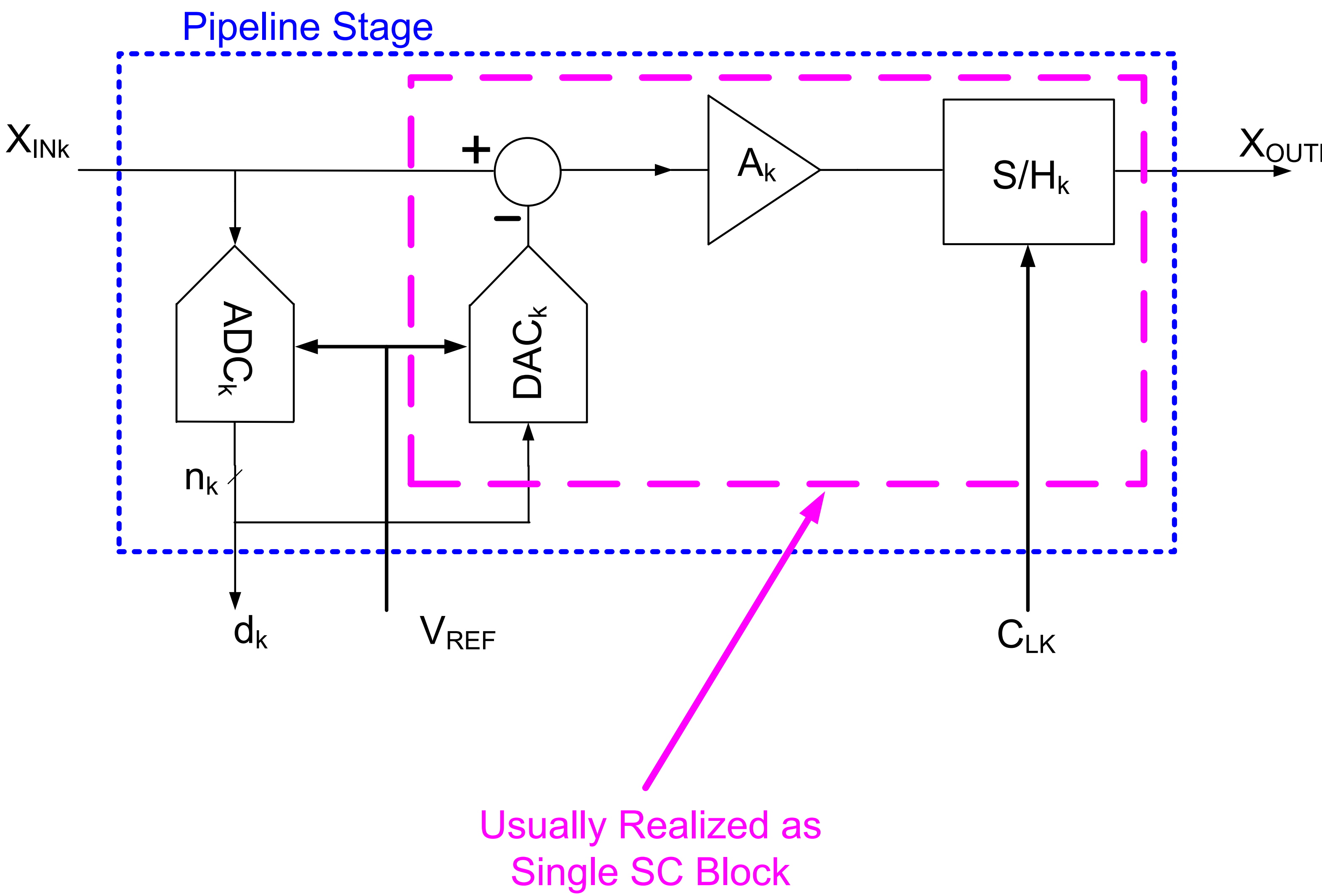
Three-Step Flash ADC with Interstage Gain





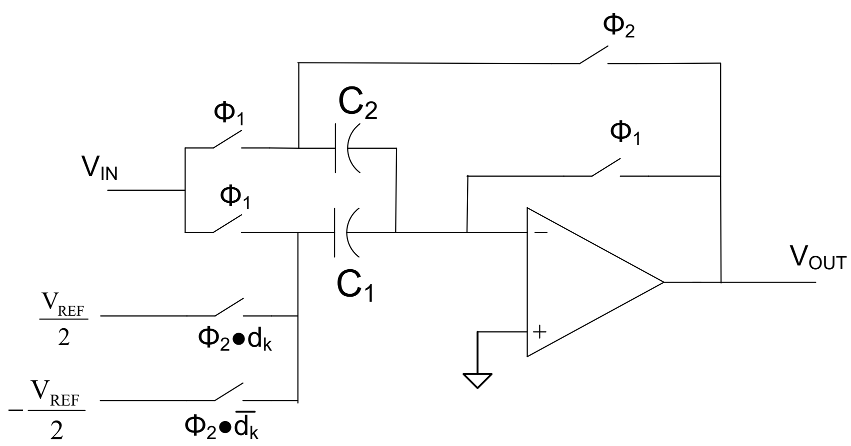
Review from Last Lecture

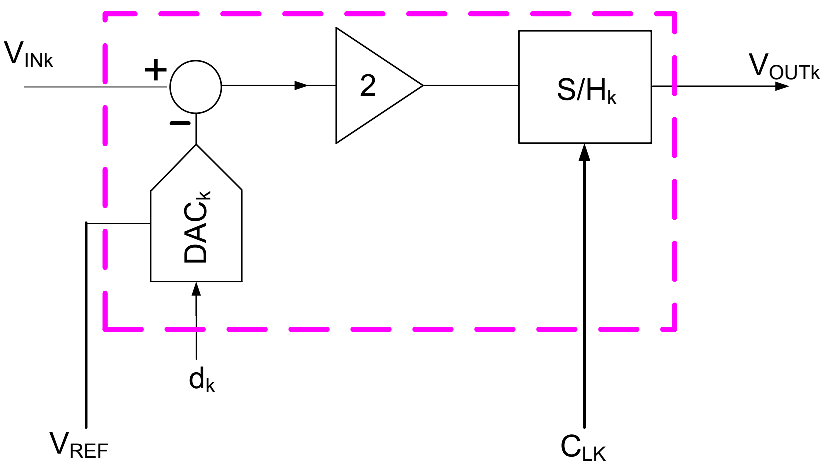
Pipelined ADC Stage k



Review from Last Lecture

1-bit/Stage Pipeline Implementation

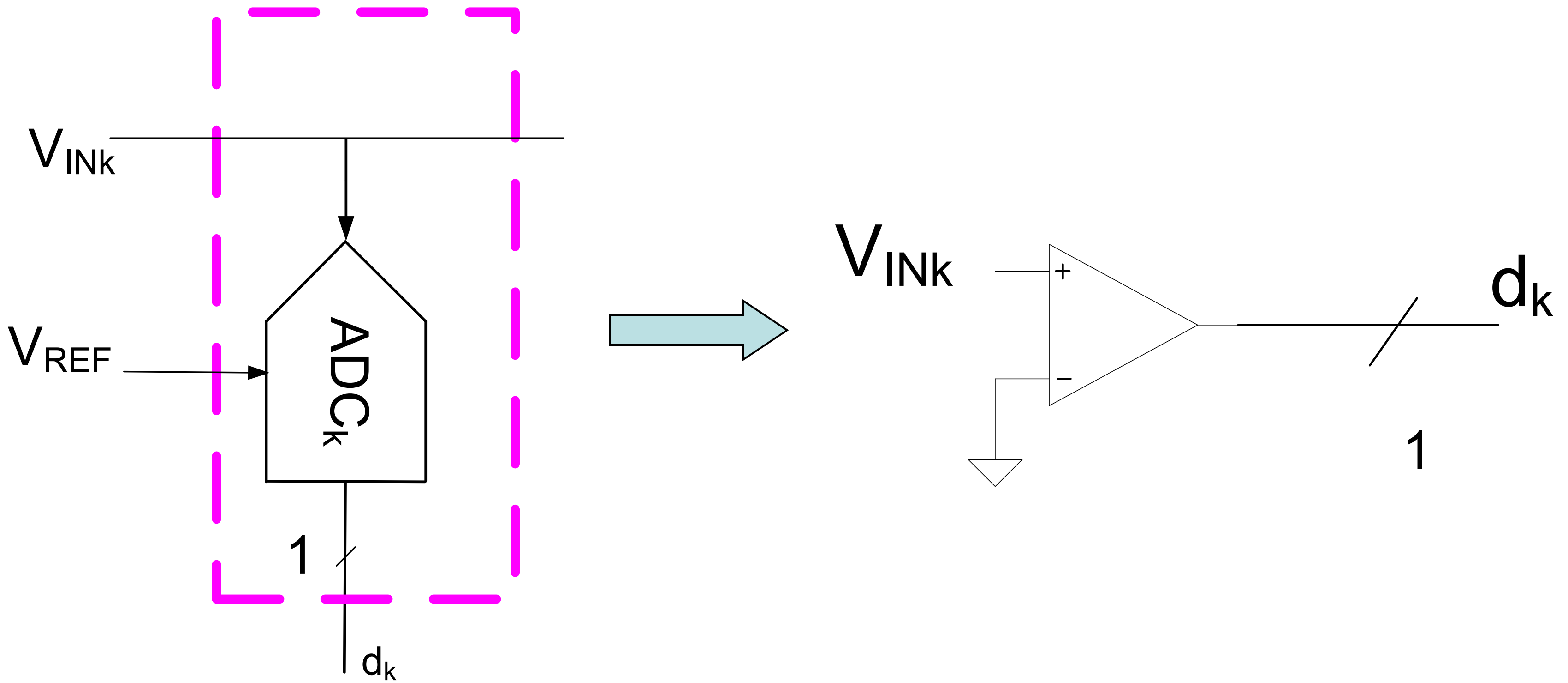




$$V_O = \begin{cases} 2V_{IN} + \dfrac{V_{REF}}{2} & V_{IN} < 0 \\ 2V_{IN} - \dfrac{V_{REF}}{2} & V_{IN} > 0 \end{cases}$$

Review from Last Lecture

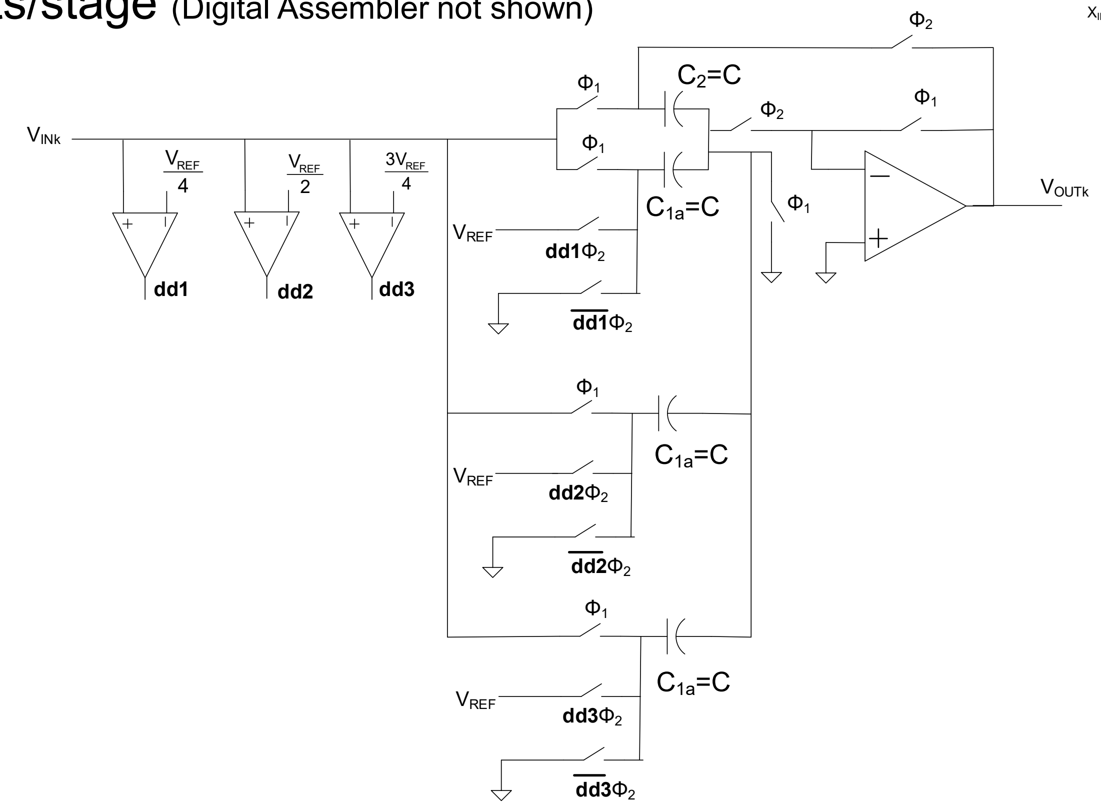
1-bit/Stage Pipeline Implementation

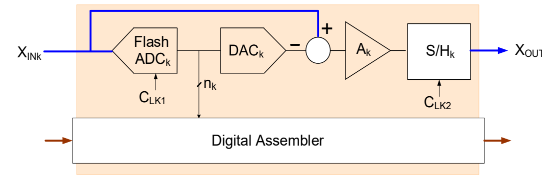


Review from Last Lecture

Typical SC Pipeline Stage

For 2 bits/stage (Digital Assembler not shown)



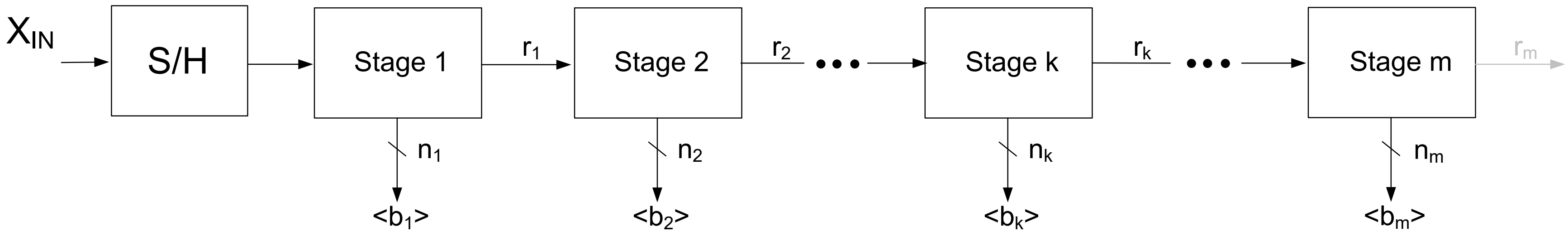


Gain =4

$$V_{OUT}=V_{IN}\left(1+\frac{C_{1a}+C_{1b}+C_{1c}}{C_2}\right)-\left(d_{d1}\left(\frac{C_{1a}}{C_2}\right)+d_{d2}\left(\frac{C_{1b}}{C_2}\right)+d_{d3}\left(\frac{C_{1c}}{C_2}\right)\right)V_{REF} \Longrightarrow V_{OUTk}=4\,V_{INk}-(d_{dd1}+d_{dd2}+d_{dd3})V_{REF}$$

- Directly use thermometer code outputs
- Can be extended to more bits/stage
- Accurate gain possible with good layout

Pipelined ADC



$X_{OUT}=<n_1:n_2:\ldots:n_m>$

- Pipelined structure is widely used
- More than one bit/stage is often used
- Optimal number of bits/stage still an area of debate
- Conceptually can simply design one stage and then copy/paste to increase resolution
- Accuracy (and correspondingly power) in latter stages can be dramatically reduced
- Most power consumed in op amps
- Power dominantly allocated to S/H and MSB stages

ADC Types

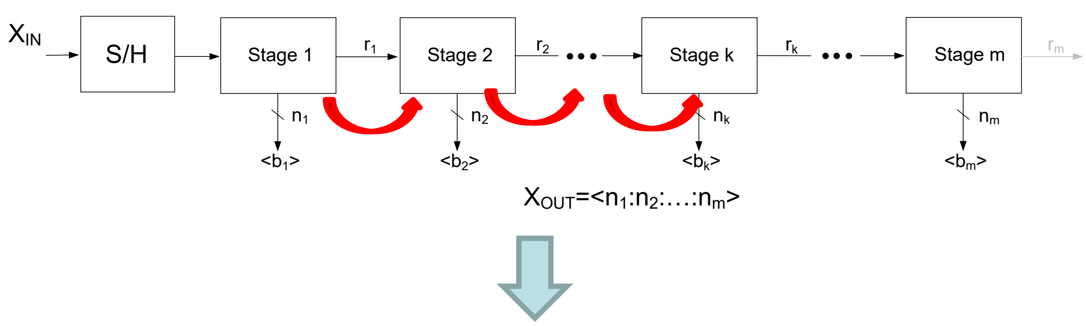
Nyquist Rate

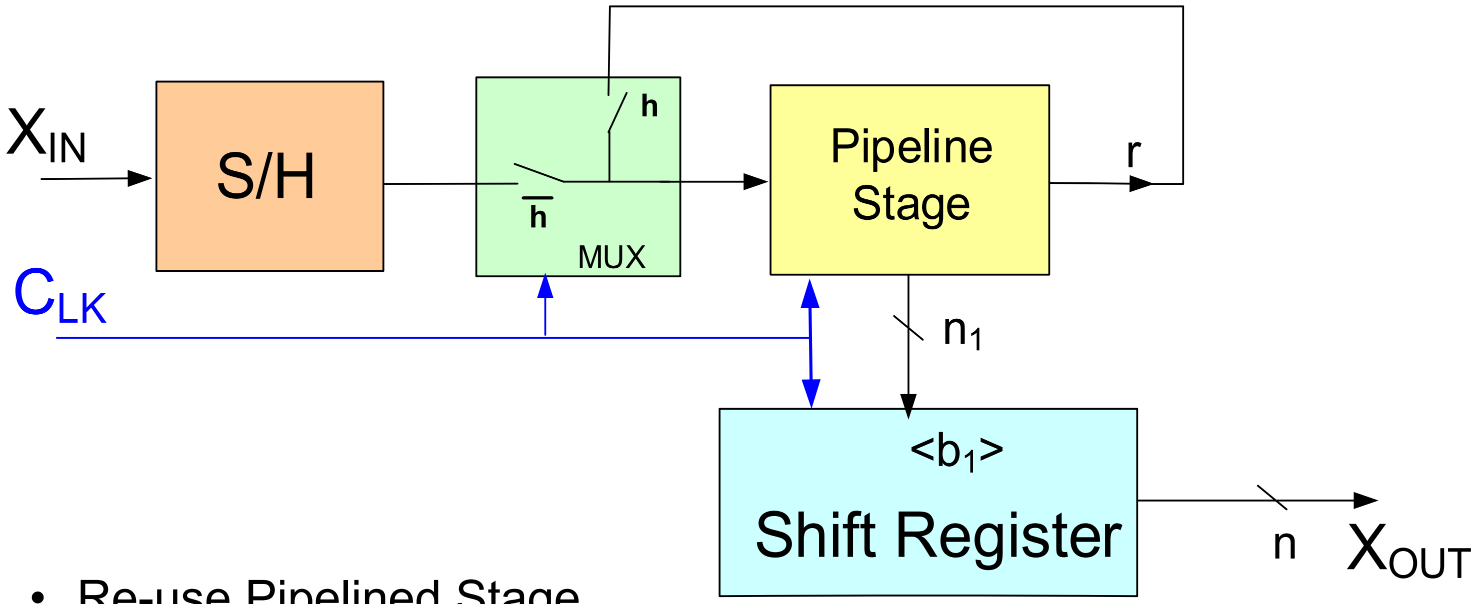
- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Interpolating
- Successive Approximation
- Folded
- Dual Slope

Over-Sampled

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

Cyclic (Algorithmic) ADC





- Re-use Pipelined Stage
- Small amount of hardware
- Effective thru-put decreases

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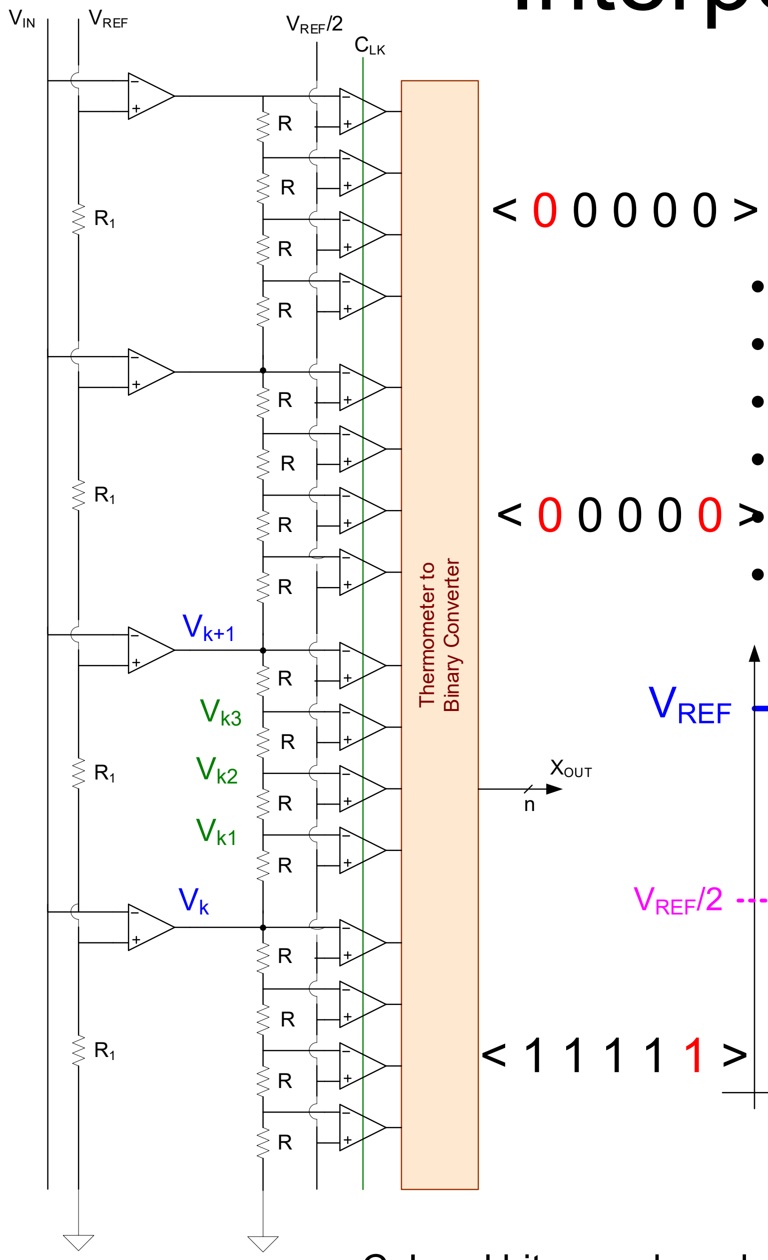
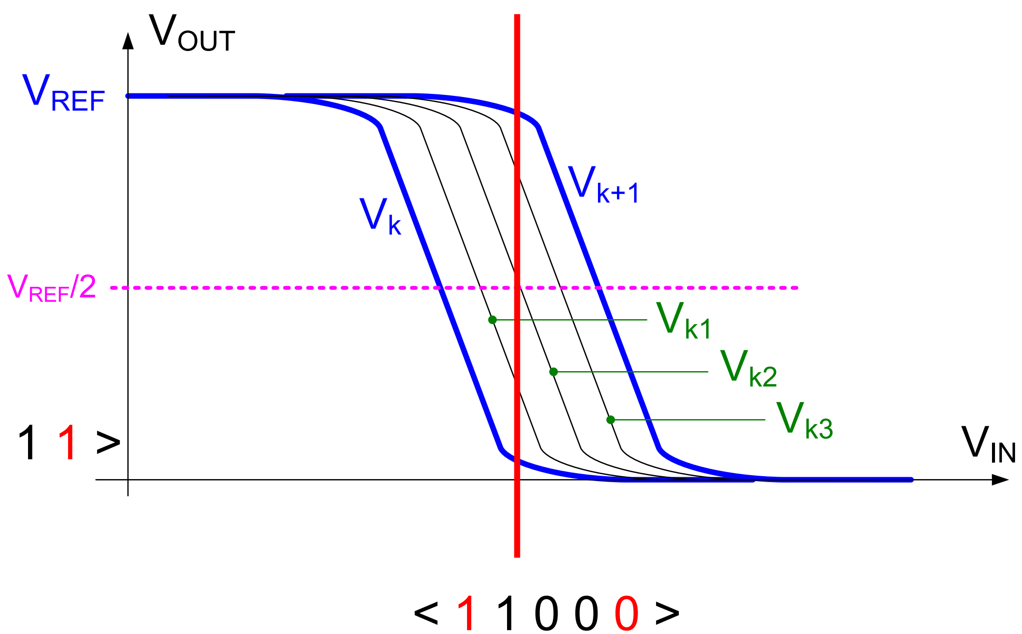
Interpolating ADC



- Amplifiers are finite-gain saturating
- Amplifiers need not be accurate or linear
- Shown for 4-bit
- Same common-mode input on comparators
- Clocked comparators usually regenerative
- Reduces Offset Requirements for Comparators



Colored bits are shared

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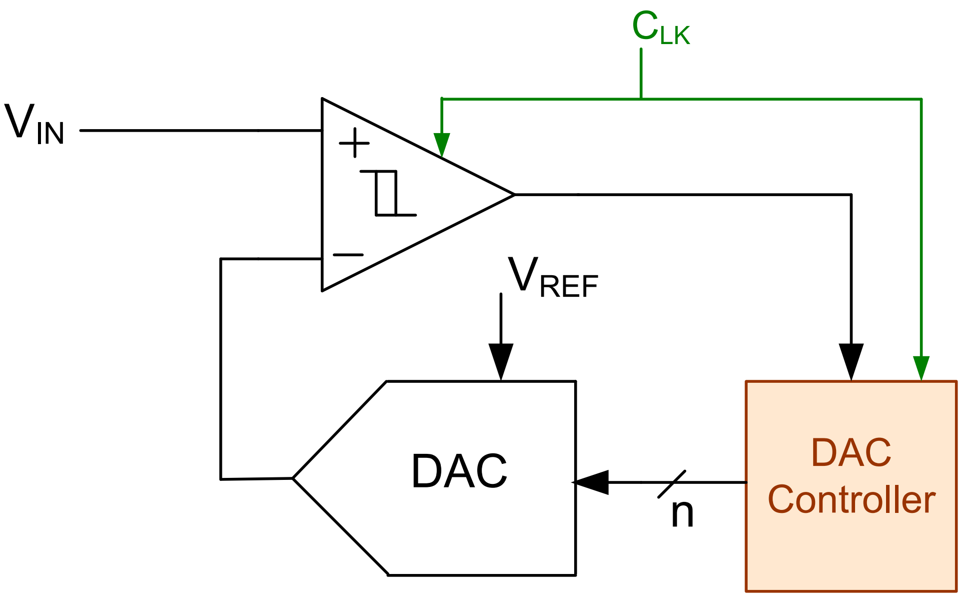
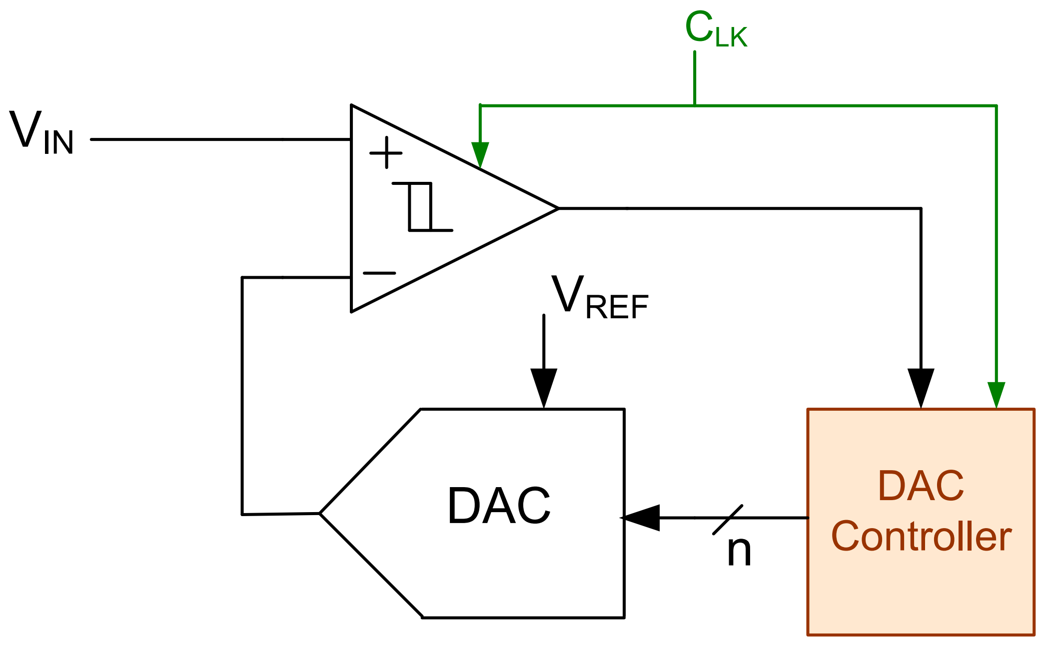
SAR ADC



ADCs
Texas Instruments

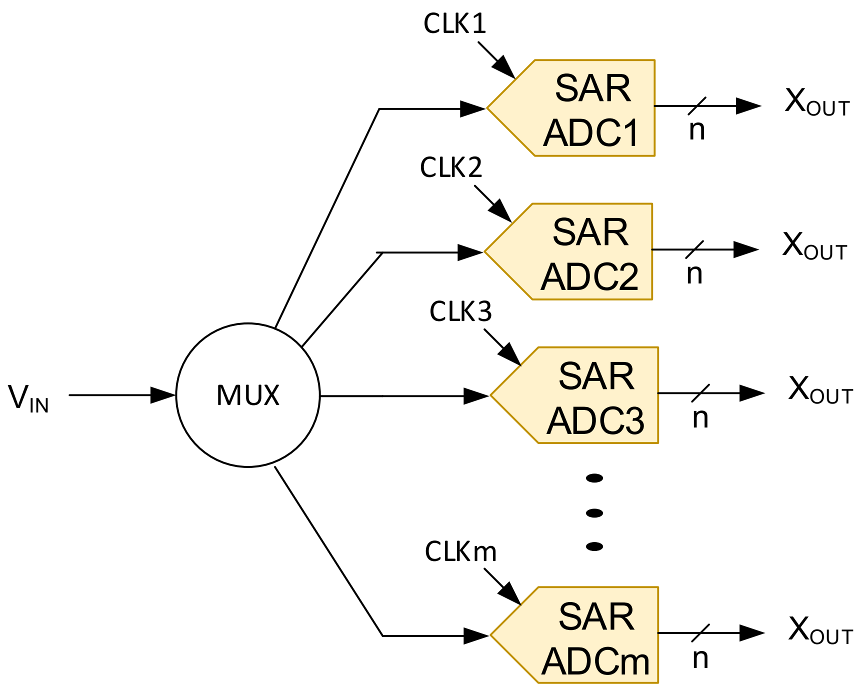
SAR	728
Pipeline	294
Delta Sigma	187
Folding Interpolating	66
Delta Sigma Modulator	9
Two-Step	6
Flash	3
Total	1293

SAR ADC

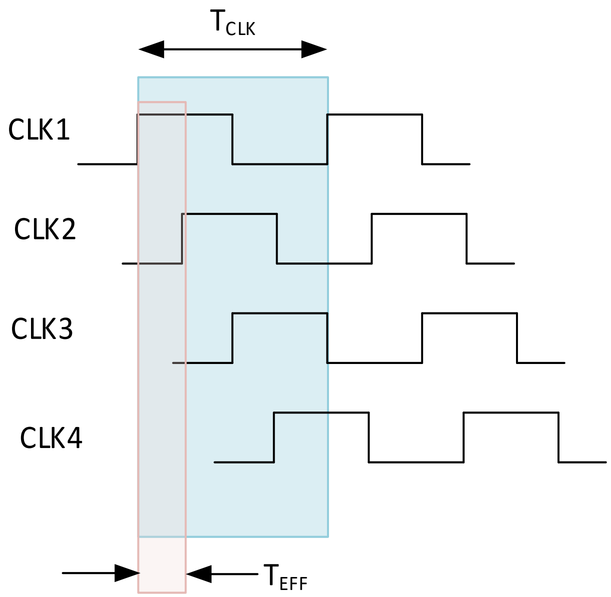


- DAC Controller may be simply U/D counter
- Binary search controlled by Finite State Machine is faster
- SAR ADC will have no missing codes if DAC is monotone
- Not very fast but can be small
- Any DAC can be used
- Single comparator !

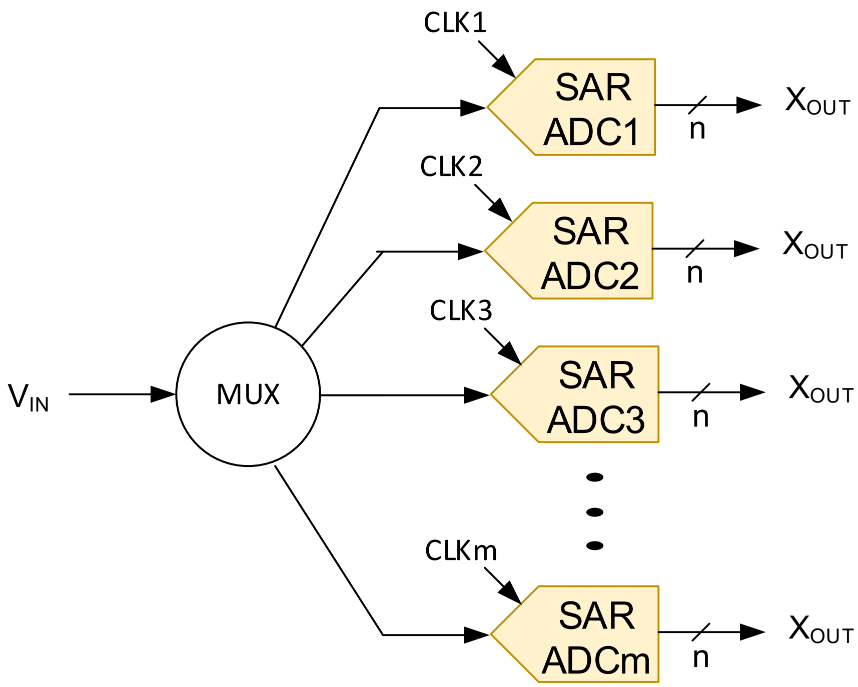
Time Interleaved SAR ADC



Time interleaving increases effective conversion rate by factor of m



Time Interleaved SAR ADC



- Provides high-speed solution when single SAR can not operate fast enough
- May be more energy efficient even is single SAR can work
- May provide better performance than pipelined structure
- Matching between stages is critical
- Clock phasing is critical
- Idea is 40+ years old but only recently has become popular
- Calibration is essential to provide matching and phasing

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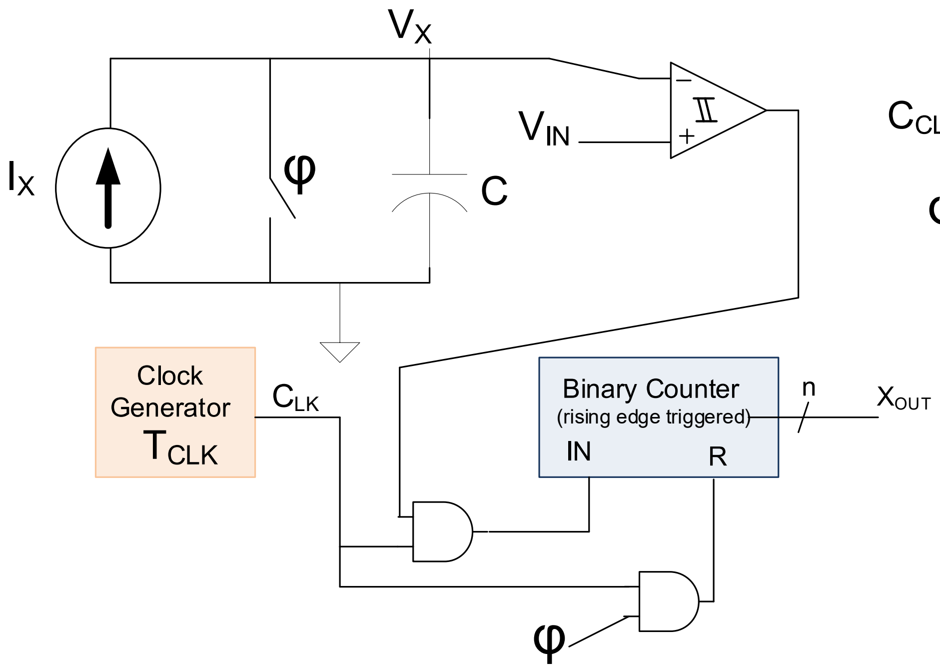
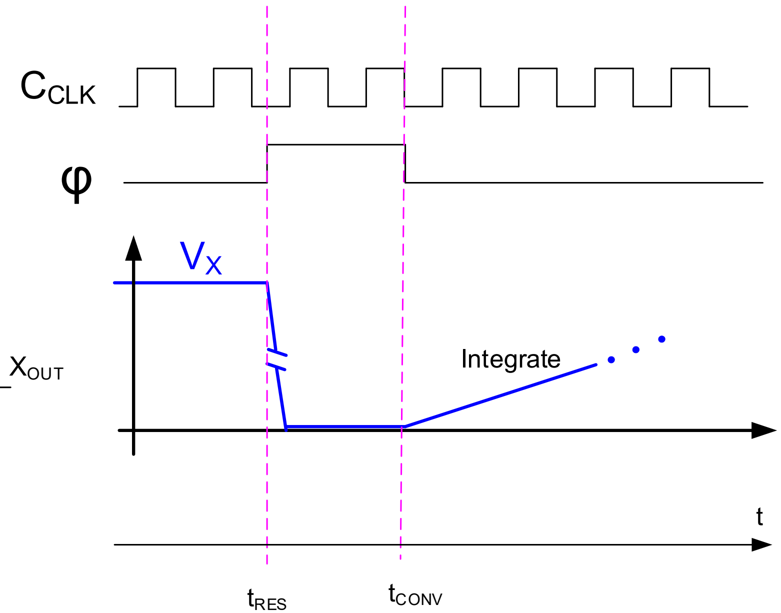
And Single Slope

Single-Slope ADC

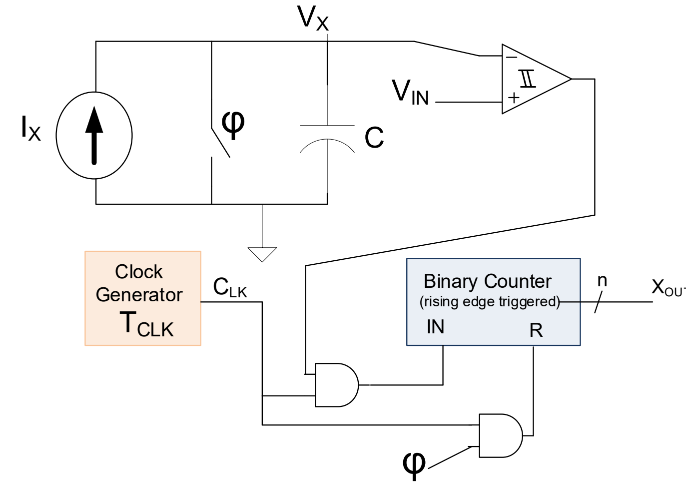
Sometimes Termed Integrating ADC





- Falling edge of φ synchronous with respect to falling edge of C_{LK}
- Can convert asynchronously wrt C_{CLK} or can be a clocked ADC where conversion clock signal is synchronous wrt C_{CLK}.
- Output valid when comparator output goes low
- Note V_{REF} not explicitly shown in ADC architecture
- Very simple structure if C is off-chip

Single-Slope ADC



Operation:

Assume $V_X(t_{CONV})=0$

$$V_X(t)=\frac{1}{C}\int_{t_{CONV}}^{t} I_X dt=\frac{I_X}{C}(t-t_{CONV}) \qquad (1)$$

Assume $I_X, V_{REF}, R, C, T_{CLK}$ are selected to satisfy the relationship

$$V_{REF}=\frac{1}{C}\int_{t_{CONV}}^{t_{CONV}+2^n T_{CLK}} I_X dt=\frac{I_X}{C}2^n T_{CLK} \qquad \text{thus} \qquad V_{LSB}=\frac{V_{REF}}{2^n}=\frac{I_X}{C}T_{CLK} \qquad (2)$$

Comparator will stop counter when $V_X=V_{IN}$ and counter output will be $X_{OUT}=k$

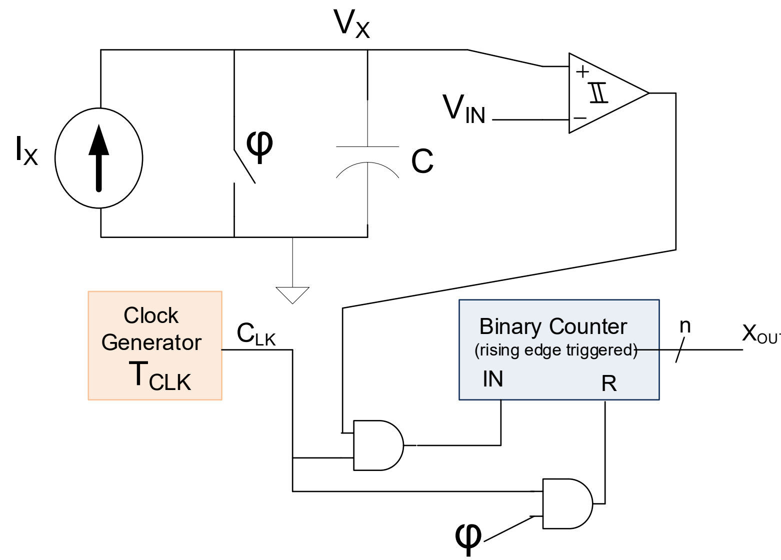
thus $V_X(t_{CONV}+kT_{CLK})=V_{IN}+\varepsilon$ where $0<\varepsilon<V_{LSB}$

It follows from (1) that

$$V_X(t_{CONV}+kT_{CLK})=\frac{I_X}{C}kT_{CLK}=V_{IN}+\varepsilon \qquad (3)$$

And finally from (2) and (3) that $V_{IN}=k\left(\frac{I_X}{C}T_{CLK}\right)-\varepsilon\cong\frac{k}{2^n}V_{REF}$

Single-Slope ADC



$I_X, V_{REF}, R, C, T_{CLK}$ must satisfy the relationship

$$V_{REF} = \frac{I_X}{C} 2^n T_{CLK} \qquad (1)$$

$$V_{IN} \cong \frac{k}{2^n} V_{REF}$$

Benefits: Very simple structure and can provide a low-cost easy solution for low speed applications

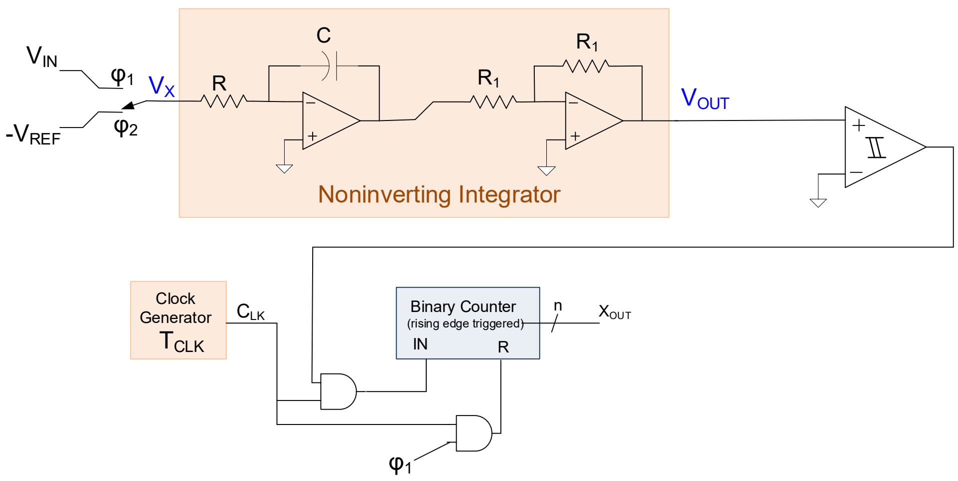
Limitations:

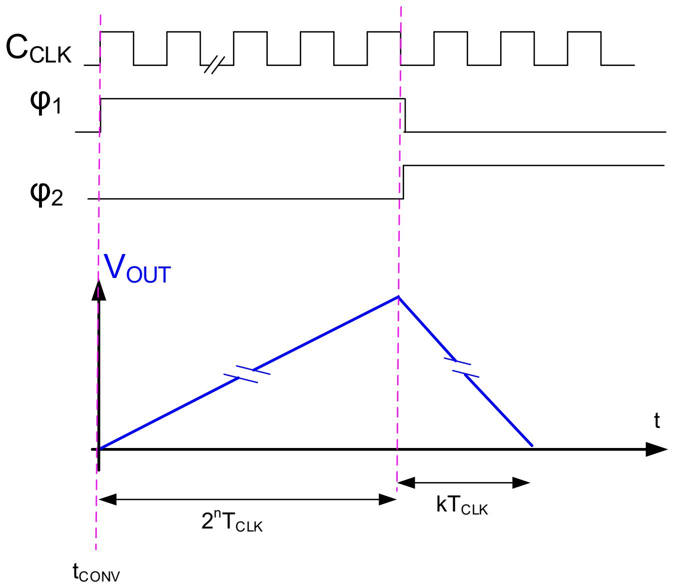
- Process variations make it difficult to satisfy (1)
- C is usually large and thus off chip is often most practical
- Linearity of C important (since often off-chip)
- Nonlinearity in I_X degrades performance
- R_{OUT} of I_X degrades performance
- Slow
- Not widely used

Options for improving performance:

- Introduce self-calibration cycle to satisfy (1) by trimming I_X or C
- Use high-impedance current source
- Use OP-Amp Based RC integrator

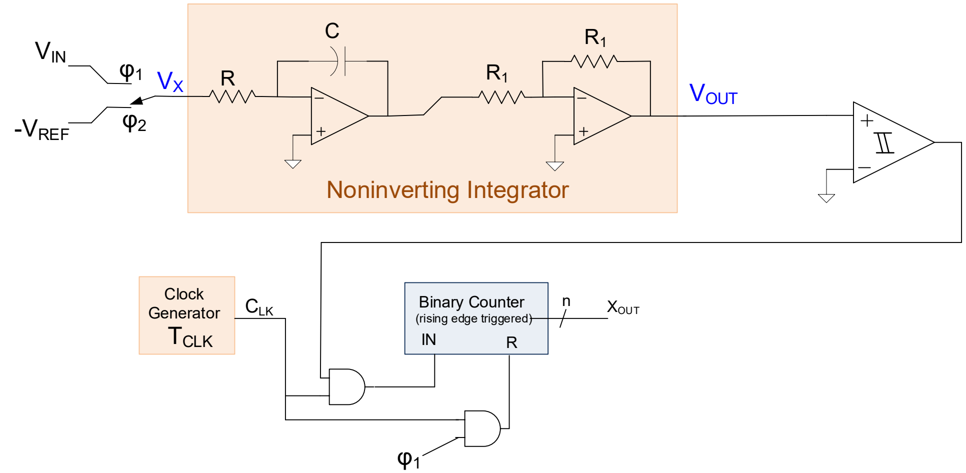
Dual-Slope ADC





- Output valid when comparator output transitions to Low
- Must set RC time constants and T_{CLK} so output does not saturate
- Shown as noninverting integrator but slight modification will also work with inverting integrator
- Other integrator structures could be used
- Can leave one or more clock cycles between integrate up and integrate down

Dual-Slope ADC



Operation:

$$V_{OUT}(t) = \frac{1}{RC}\int_{t_{CONV}}^{t} V_X dt$$

During φ_1, integrate V_{IN} for time $2^n T_{CLK}$

At end of integrate up interval, $V_{OUT}\left(2^n T_{CLK}\right) = \frac{1}{RC} V_{IN} 2^n T_{CLK}$

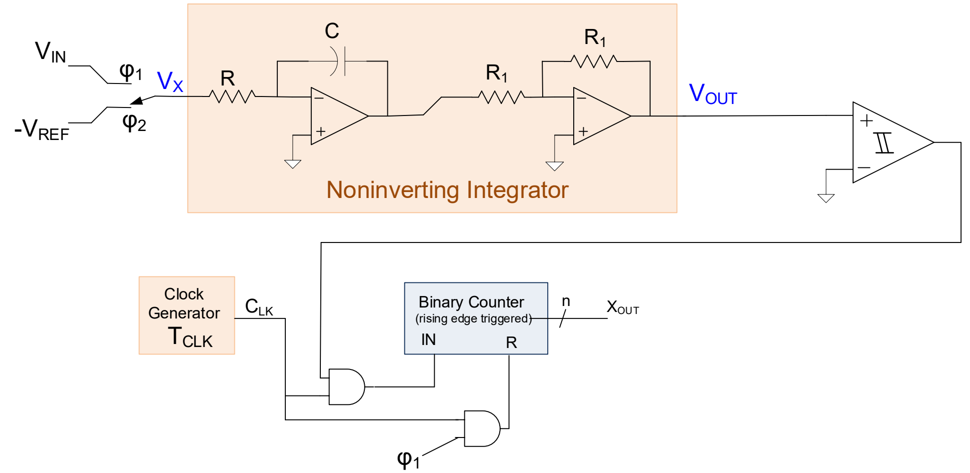
Reset counter at time $2^n T_{CLK}$

During φ_2, integrate $-V_{IN}$ until comparator goes low and count clock transitions during down integration interval. At time comparator changes states, $V_{OUT}=0$ and code in counter is k

$$0 = \frac{1}{RC}\int_{t_{CONV}}^{t_{CONV}+2^n T_{CLK}} V_{IN} dt - \frac{1}{RC}\int_{t_{CONV}+2^n T_{CLK}}^{t_{CONV}+2^n T_{CLK}+kT_{CLK}} V_{REF} dt \quad \Rightarrow \quad \frac{1}{RC} V_{IN} 2^n T_{CLK} = \frac{1}{RC} V_{REF} k T_{CLK}$$

Solving, obtain: $V_{IN} = \frac{k}{2^n} V_{REF}$

Dual-Slope ADC



$$V_{IN} = \frac{k}{2^n} V_{REF}$$

Observations:

Benefits

- Not dependent upon R, C, or T_{CLK} (provided integrator does not saturate)
- Very simple structure that can give good results and cost can be low
- Inherently monotone

Limitations:

- Capacitor large and likely must be off-chip
- Linearity of capacitor is important (particularly of concern when off-chip)
- Slow
- Not widely used

Stay Safe and Stay Healthy !

End of Lecture 37